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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/686,090	10/12/2000	Toshiyuki Oda	Q61276	5198

7590 03/31/2004

SUGHRUE, MION, ZINN, MACPEAK & SEAS
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EXAMINER	
JACKSON, BLANE J	

ART UNIT	PAPER NUMBER
2685	

DATE MAILED: 03/31/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/686,090	ODA, TOSHIYUKI	
	Examiner	Art Unit	
	Blane J Jackson	2685	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 January 2004* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 01/20/04 have been fully considered but they are not persuasive as regards claims 1, 3, 5, 7 and 8 but the claims are modified for clarity as regards means for controlling the control timing. However, new grounds of rejection in view of Poutanen U.S. Patent 5,457,813 are made for claims 2, 4 and 6.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 3, 5 and 7-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rainish et al. (U.S. Patent 6,606,490) with a view to Hideo (JP-A 10-200353).

As to claim 1, Rainish teaches an AGC circuit in a CDMA receiver comprising an AGC loop for calculating received signal power level from a received signal and controlling the received signal power level to be constant (figures 3 - 5, column 3, lines 3-41, Rainish determines whether or not to utilize AGC based on threshold comparisons of the signal power measurement during a pre conditioning interval). Rainish does not include means for controlling the control timing based on control amount.

Hideo teaches a AGC control method for a receiver where the AGC operation mode, the AGC signal, is established at a point of time a little before the arrival of the next burst receiving timing by estimation of the startup time in relation to the following slot and changing the gain control initiation timing to be earlier than the following slot head (Abstract, figure 7 and paragraph 0049, as represented in a copy of a Japanese Office Action dated March 19, 2003 from the applicant's IDS).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the AGC system of Rainish with the AGC circuit under timing control of Hideo to ensure an operating and satisfactory AGC control from the first part of the burst (the beginning of the slot with data information) signal.

As to claim 3, Rainish teaches a CDMA demodulator for receiving and demodulating a spread spectrum signal (figure 3) comprising an AGC loop including an intermediate frequency signal converter (downconverter (102)) for converting the spread spectrum signal to an intermediate frequency signal and an AGC amplifier ((103) & (105)) for variable gain amplifying the intermediate frequency signal with a control voltage (column 2, lines 1-20), and

the AGC loop includes a power level calculating unit for calculating the level of full power in the band of a channel under reception (Rx power estimator (124), column 2, lines 11-20 and column 3, lines 25-35). Rainish also teaches the power level calculating unit starting the power level calculation from an instant corresponding to the

forefront of a slot (figure 2-prior art, period Tagc shows AGC operation in the forefront of a slot prior to the assigned data slot and figure 4, section Trfb2).

As to claim 5, with reference to claims 3 or 4, Rainish does not teach where the AGC includes a control unit for calculating control time according to the result of calculation in the power level calculating unit, calculating and controlling the control timing based on the control amount and feeding out the control voltage.

Hideo teaches a controller (figure 1, (10)) that outputs a reception discrimination signal for designating the AGC operation mode at a point of time a little before the arrival of the next burst receiving timing (timing to estimate the startup time to prepare the AGC level in relation to the following data slot) where the determined control amount is based on the reception signal intensity detected by the level detector (5) (figure 7 and Abstract and paragraph 0049). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the AGC system of Rainish with the timing control of Hideo to present a stable or satisfactory AGC level at the start of the following data slot.

As to claim 7, Rainish teaches a CDMA demodulator for receiving and demodulating a spread spectrum signal (figures 1 & 3, column 2, lines 1-41) comprising:

An intermediate frequency signal converter for receiving the spread spectrum signal and converting the same signal to an intermediate frequency signal (downconverter (102)),

An AGC amplifier for variable gain amplifying the intermediate frequency signal with a control voltage (AGC 1 (103) and AGC 2 (106) distributed with a bandpass filter included),

A demodulating unit for demodulating the output signal of the AGC amplifier to a base-band signal (quadrature type, mixers (108), (109),

A first low pass filter for limiting the band of the base-band signal to a band corresponding to one channel and feeding out a first low-pass filter output signal (LPFs (110), (111),

An A/D converter for quantizing the level of full power in the band of the first low-pas filter output signal and feeding out the quantized signal (A/D converters (112), (113),

A power level calculating unit for averaging the power level of the quantized signal for a predetermined period of time from an instant corresponding to the forefront of slot and feeding out an average power level signal representing the average power level (Rx power estimator (124), reference claim 3 for discussion as to forefront of a slot),

Rainish does not teach a control unit for calculating control time based on the average power level represented by the average power level signal and feeding out control data upon reaching of a predetermined instant of time. Rainish exhibits a circuit that necessarily includes but is silent as to an A/D converter for converting the control data to an analog control signal and a second low-pass filter for waveform shaping the along control signal and feeding the control voltage to the AGC amplifier.

Hideo teaches a digital wireless receiver with an AGC loop (figure 1, (4)) that includes a D/A converter (8) for converting control data followed by a low pass filter (9) to feed the control voltage to the AGC amplifier (3). It would have been obvious to one of ordinary skill in the art at the time of the invention to realize in Rainish the loop components shown by Hideo to complete a functioning AGC control loop between the control amount determination and variable RF amplifier.

Hideo further teaches a control unit (10) for calculating control time based on the average power level represented by the average power level signal and feeding out control data upon reaching of a predetermined instant of time (Abstract and per admission in applicant's IDS reference of a Japanese Office Action dated March 19, 2003). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the AGC system of Rainish with the timing control of Hideo to present a stable or satisfactory AGC level at the start of the following data slot.

As to claims 8 and 9, Rainish teaches a method for controlling the timing of an AGC circuit in a receiver in which signals are received during a plurality of independent slots (figure 3, column 3, lines 1-14), the method comprising:

Calculating the average power of a received signal corresponding to a first slot (figures 4 and 5, column 3, lines 25-35, lines 52-67),

Initiating an AGC control of the second slot based on the calculated average power received in the first slot (column 3, lines 14-24),

Wherein the AGC control of the second slot is initiated at a time prior to a beginning of the second slot (figure 4, Tagc prior to slot Tdec).

Rainish does not directly teach but shows an understanding of determining a rise time of the AGC circuit specifically with respect to a second slot wherein the AGC control of the second slot is initiated at a time prior to a beginning of the second slot based on the rise time or beginning of the second slot. Rainish teaches power measurement and AGC control in a pre-conditioning slot followed by "sleep" time well prior to the second or forthcoming data slot to be demodulated as shown in figure 4. Hideo teaches designating an AGC operation mode at a point of time a little before the arrival of the next burst receiving timing, the instant of start of control is variably set, with a gain setting from the AGC control sets the gain of a variable gain amplifier based on reception signal intensity detected by a reception level detector in the AGC operation mode (Abstract). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to recognize in Rainish the AGC control details of Hideo for satisfactory AGC control, ready and stable, from the first part of the signal to be received.

As to claim 10, Rainish teaches a method with respect to claim 9 wherein the AGC control results in the respective power levels of the first and second slots being equal (the result of automatic gain control, column 3, lines 25-35).

4. Claims 2, 4, 6 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rainish et al. (U.S. Patent 6,606,490) with a view to Poutanen (U.S. Patent 5,457,813).

As to claims 2 and 11, Rainish teaches a CDMA demodulator for receiving and demodulating a spread spectrum signal comprising:

An AGC loop including an intermediate frequency signal converter for converting the spread spectrum signal to an intermediate frequency signal (figures 1 & 3, column 2, lines 1-29),

An AGC amplifier for variable gain amplifying the intermediate frequency signal with a control voltage (figure 3, AGC (103) and AGC2 (106)),

Rainish also teaches the AGC includes a power level calculating unit (column 3, lines 4-35) but does not teach a power level calculating unit operable to calculate the level of full power in the band of a channel under reception by averaging the receive power over a predetermined time period.

Poutanen teaches a method to realize both automatic gain control and automatic power control at mobile stations in a CDMA network (column 1, lines 41-65) where the power level calculating unit is operable to calculate the level of full power in the band of a channel under reception by averaging the receive power over a predetermined period (column 2, line 61 to column 3, line 25). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the AGC circuit of Rainish with the alternative control as taught by Poutanen such that the setpoint value of AGC is calculated from the received information signal without extra pilot signals.

As to claim 4, Rainish teaches the claim elements discussed in claim 3 but does not teach the AGC loop includes a power level calculating unit making the length of the subject of calculation to be variable.

Poutanen teaches a CDMA demodulator for receiving and demodulating a spread spectrum signal comprising an AGC loop that includes a power level calculating unit (figure 1, Automatic Gain Control (7)) for calculating the level of full power in the band of a channel under reception, the power level calculating unit making the length of the subject of calculation to be variable (column 2, lines 11-30 and column 2, line 61 to column 3, line 14). It would have been obvious to one of ordinary skill in the art at the time of the invention to alter the power measurement system of Rainish with the variable method taught by Poutanen to be performed independent of the mobile station and without loading the radio network.

As to claim 6, with respect to claim 2, Rainish teaches the power level calculating unit starts the power level calculation from an intermediate part of the slot (figures 4 and 5, where the system selects full AGC operation after a short received signal power measurement during the "pre-conditioned interval" prior to sleep and start of the next slot to be received, column 3, lines 25-35).

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Blane J Jackson whose telephone number is (703) 305-5291. The examiner can normally be reached on Monday through Friday, 8:00 AM-5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Urban can be reached on (703) 305-4385. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BJJ

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